

User's Guide

NHD-12864**MZ-FSW-GBW-L**

LCM

(Liquid Crystal Graphic Display Module)

RoHS Compliant

NHD = Newhaven Display

128 x 64 = Pixels

MZ = Version

F = Transflective (+)

S, W = Side White LED Backlight

G = STN-Gray

B = 6:00 View

W = Wide Temperature -20 ~ +70c

L = Low Current Option

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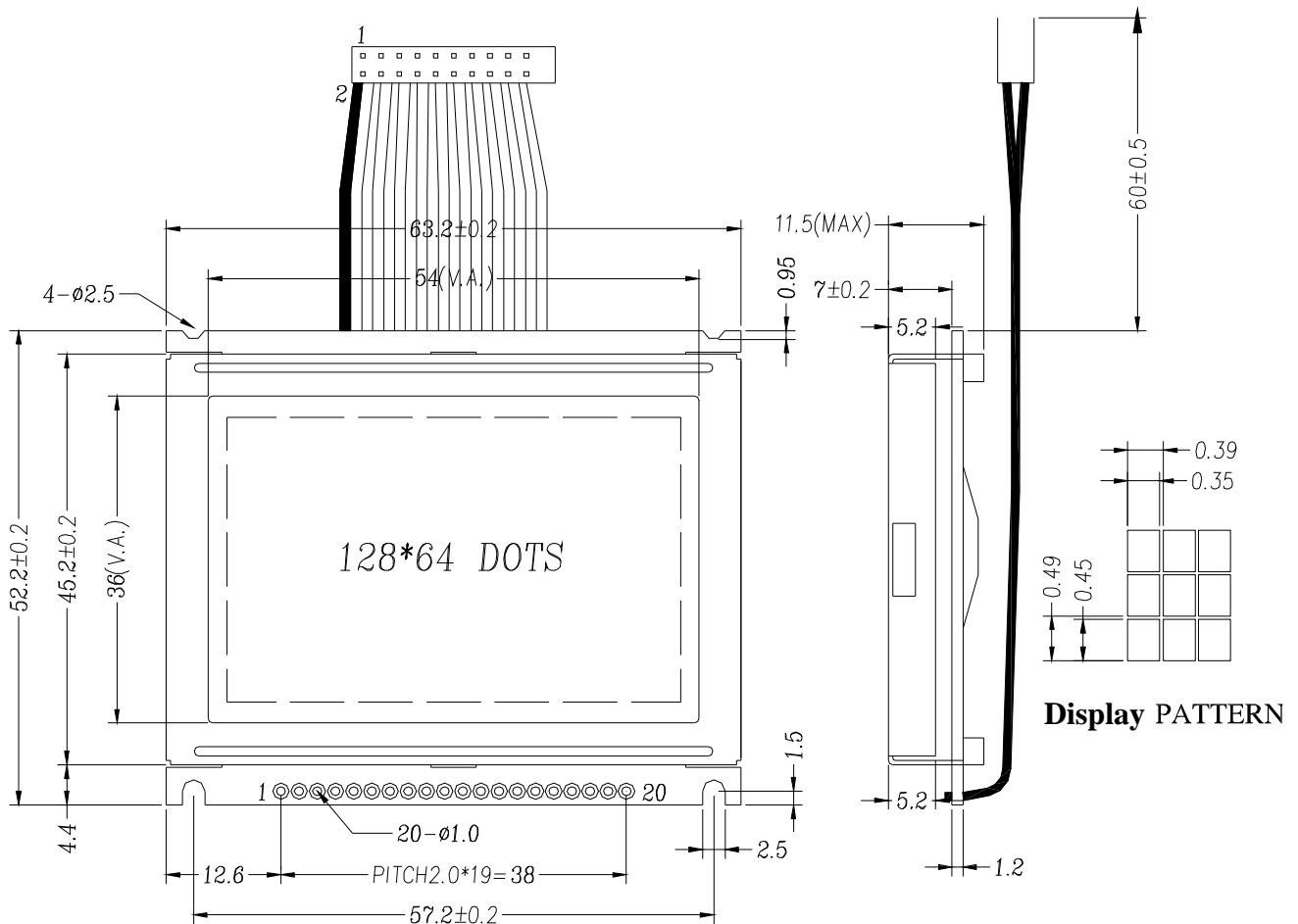
NHD-12864MZ-FSW-GBW-L SPECIFICATION OF LCD MODULE

NHD-12864MZ is a dot matrix graphic LCD module which is fabricated by low power COMS technology. It can display 128*64 dots size LCD panel using a 128*64 bit-mapped Display Data RAM (DDRAM). It interfaces with an 8-bit microprocessor.

Features

- | Display format: 128*64 dots matrix graphic
- | STN GRAY mode
- | Easy interface with 8-bit MPU
- | Low power consumption
- | LED Side-light (WHITE)
- | Viewing angle: 6 O'clock
- | Driving method: 1/64 duty, 1/9 bias
- | LCD driver IC: KS0108B、KS0107B
- | Connector: zebra

Outline dimension



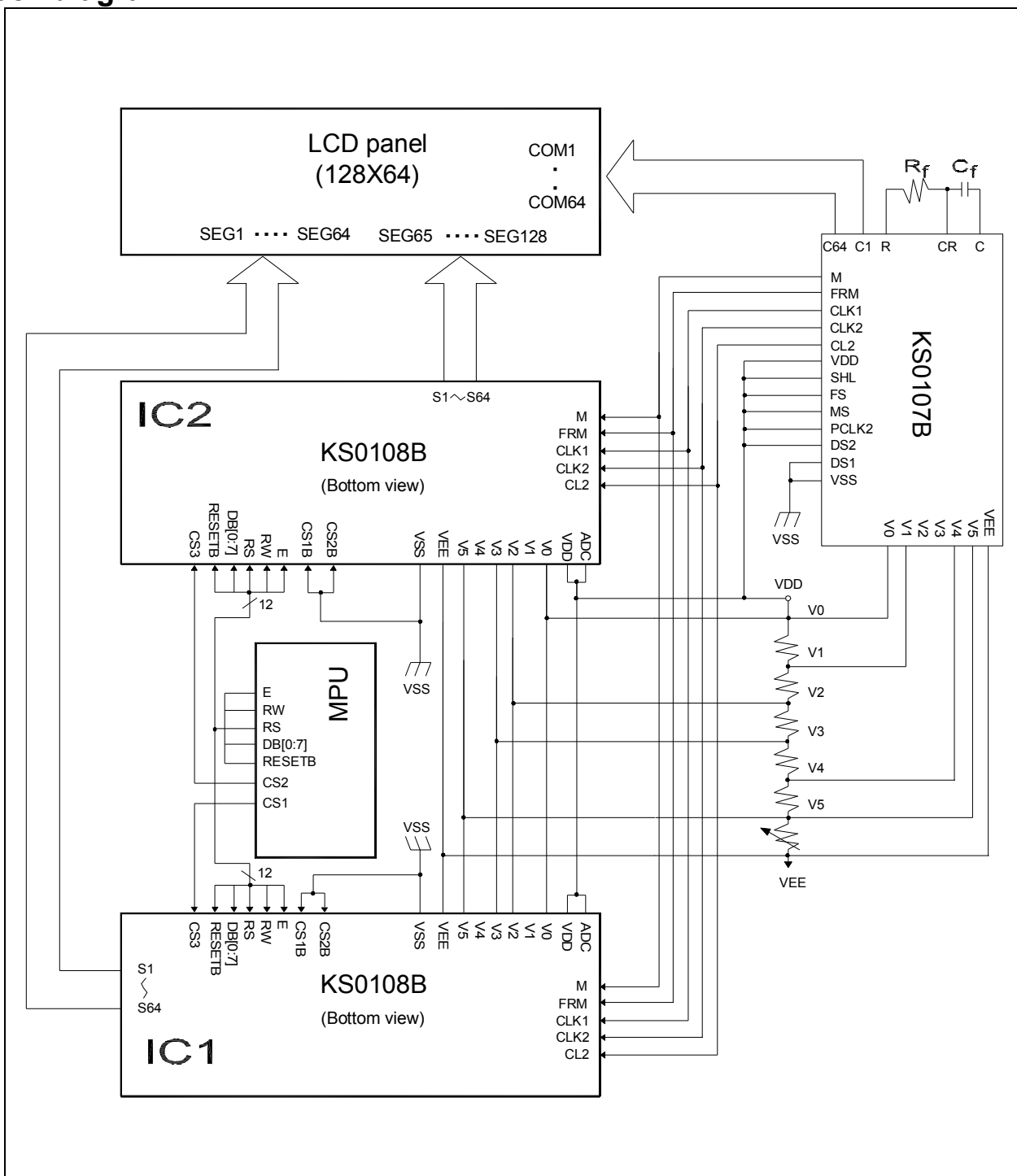
INTERFACE PIN CONNECTIONS

PIN NO	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SIGNAL	VDD	VSS	V0	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	CS2	CS1	RST	R/W	D/I	E	VSS	A	K

Absolute maximum ratings

Item	Symbol	Standard	Standard	Unit
Power voltage	$V_{DD}-V_{SS}$	0	-	7.0
Input voltage	V_{IN}	V_{SS}	-	V_{DD}
Operating temperature range	V_{OP}	-20	-	+70
Storage temperature range	V_{ST}	-30	-	+80

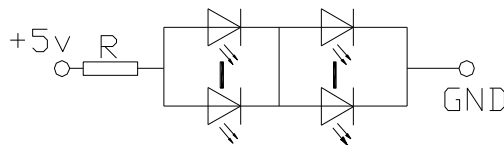
Block diagram



Interface pin description

Pin no.	Symbol	External connection	Function
1	V _{DD}	Power supply	Power supply for logic (+5V) for LCM
2	V _{SS}		Signal ground for LCM (GND)
3	V ₀		Contrast adjust
4~11	DB0~DB7	MPU	Data bus [0~7] Bi-directional data bus
12	CS2	MPU	Chip selection: When CS1=H,CS2=L, select IC1 When CS1=L,CS2=H, select IC2
13	CS1	MPU	
14	RST	MPU	Reset signal. When RSTB=L
15	R/W	MPU	Read/write select signal
16	D/I		Register select signal
17	E		Operation (data read/write) enable signal
18	VSS		Signal ground for LCM (GND)
19	A	LED BKL Power supply	Power supply for BKL (+5V)
20	K		Power supply for BKL (GND)

Backlight circuit diagram(light 2X30)



LED ratings

(voltage= 5V,R=51 Ω)

Item	Symbol	Min	Typ.	Max	Unit
Forward Voltage	V _F	3.1	3.3	3.5	V
Forward current	I _F	-	33		mA
Power	P			180	mW
Peak wave length	λ _p		568		nm
Luminance	L _v		200		Cd/m ²

Optical characteristics

STN type display module (Ta=25℃, VDD=5.0V)

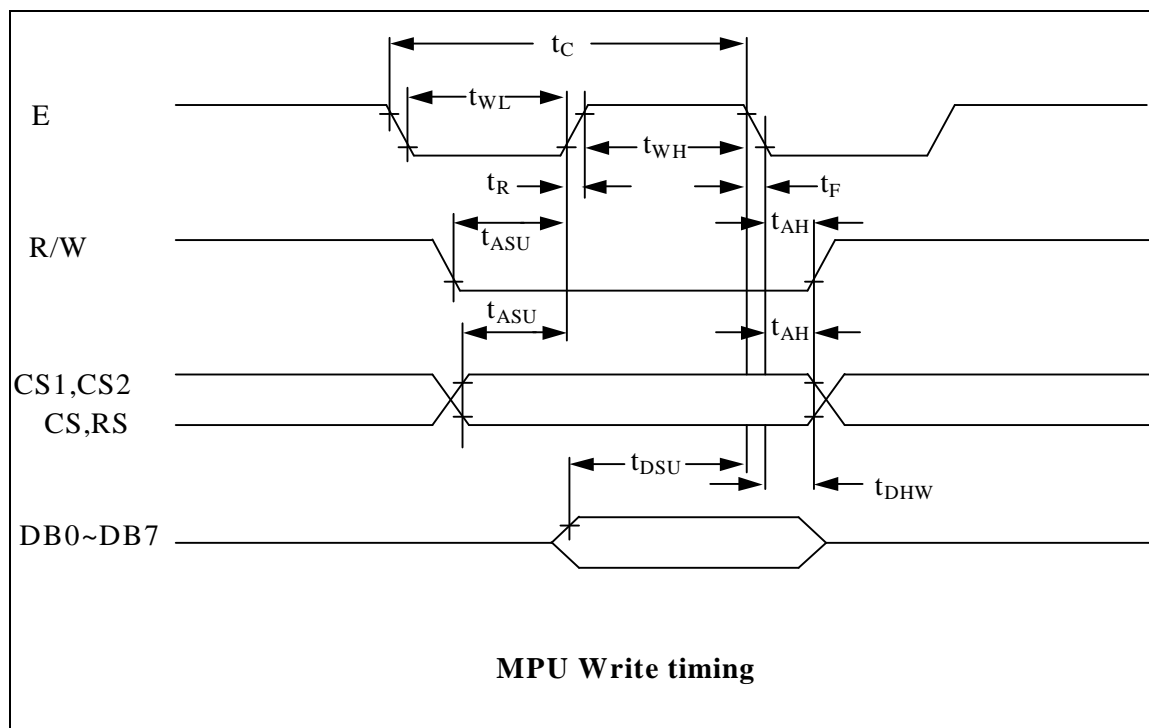
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle	θ	C _r ≥ 2	-60	-	35	deg
	Φ		-40	-	40	
Contrast ratio	C _r		-	6	-	-
Response time (rise)	T _r	-	-	150	250	ms
Response time (fall)	T _r	-	-	150	250	

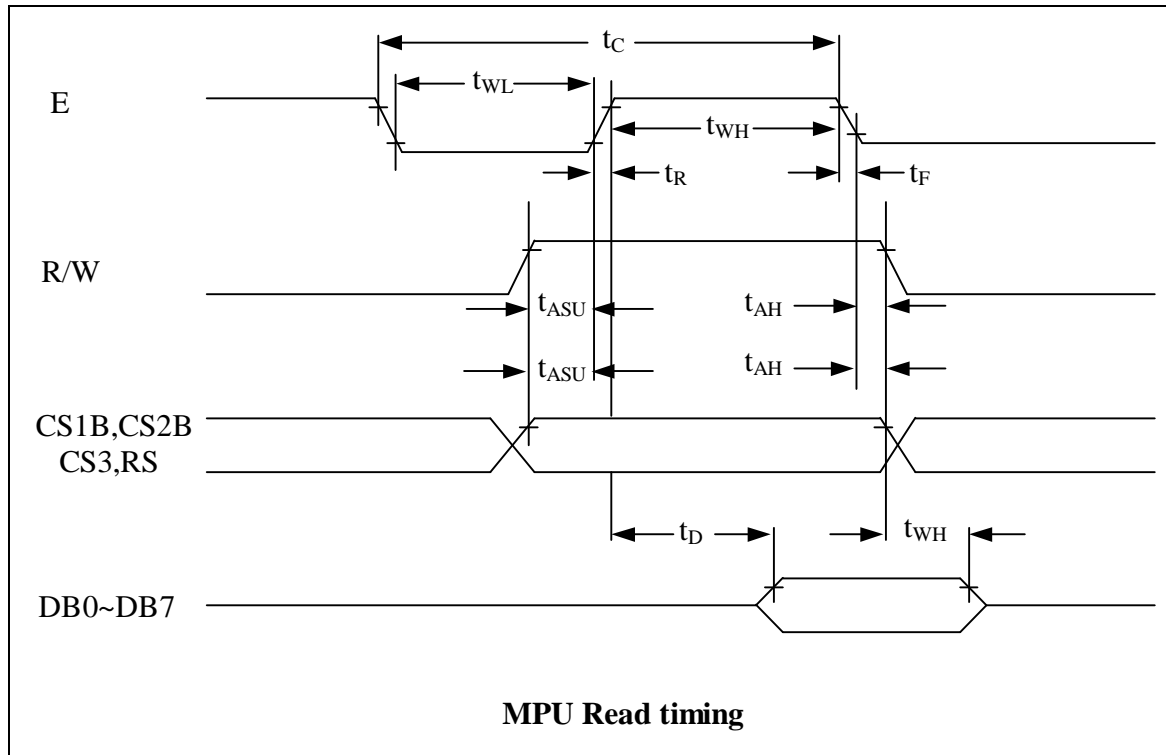
DC Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage for LCD	$V_{DD}-V_0$	$T_a=25^{\circ}C$	-	13.8	-	V
Input voltage	V_{DD}		4.7	-	5.5	
Supply current	I_{DD}	$T_a=25^{\circ}C, V_{DD}=5.0V$	-	0.41		mA
Input leakage current	I_{LKG}		-	-	1.0	uA
“H” level input voltage	V_{IH}		2.2	-	V_{DD}	V
“L” level input voltage	V_{IL}	Twice initial value or less	0	-	0.6	
“H” level output voltage	V_{OH}	LOH=-0.25mA	2.4	-	-	
“L” level output voltage	V_{OL}	LOH=1.6mA	-	-	0.4	
Backlight supply voltage	V_F		-	3.4	3.6	
Backlight supply current	I_F	$V=5.0V R=51\ \Omega$	-	33		mA

MPU Interface

Characteristic	Symbol	Min	Typ	Max	Unit
E Cycle	t_C	1000	-	-	ns
E High Level Width	t_{WH}	450	-	-	
E Low Level Width	t_{WL}	450	-	-	
E Rise Time	t_R	-	-	25	
E Fall Time	t_F	-	-	25	
Address Set-Up Time	t_{ASU}	140	-	-	
Address Hold Time	t_{AH}	10	-	-	
Data Set-Up Time	t_{SU}	200	-	-	
Data Delay Time	t_D	-	-	320	
Data Hold Time (Write)	t_{DHW}	10	-	-	
Data Hold Time (Read)	t_{DHR}	20	-	-	





OPERATING PRINCIPLES & METHODS

1. I/O Buffer

Input buffer controls the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS1B-CS3.

2. Input register

Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display RAM.

When CS1B to CS3 are in the active mode, R/W and RS select the input register. The data from MPU is written into input register. Then writing it into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

3. Output register

Output register stores the data temporarily from display data RAM when CS1B, CS2B and CS3 are in active mode and R/W and RS=H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W=H, RS=L, status data (busy check) can read out.

To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

RS	R/W	Function
L	L	Instruction
	H	Status read (busy check)
H	L	Data write (from input register to display data RAM)
	H	Data read (from display data RAM to output register)

4. Reset

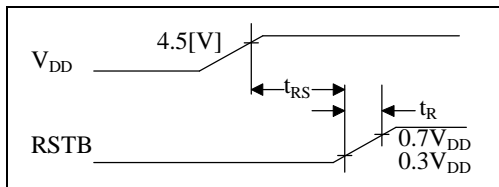
The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU. When RSTB becomes low, following procedure is occurred.

1. Display off
2. Display start line register become set by 0.(Z-address 0)

While RSTB is low, No instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4= (clear RSTB) and DB7=0 (ready) by status read instruction. The conditions of power supply at initial power up are shown in table 1.

Table 1. Power Supply Initial Conditions

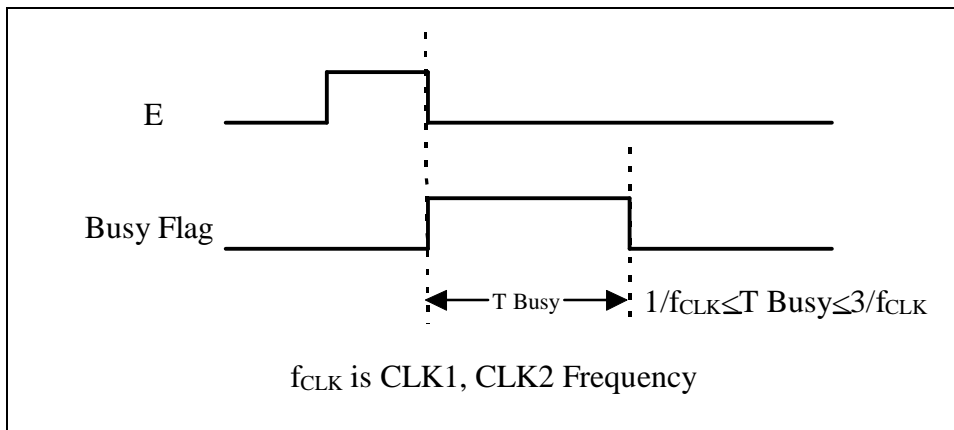
Item	Symbol	Min	Typ	Max	Unit
Reset Time	t_{RS}	1.0	-	-	us
Rise Time	t_R	-	-	200	ns



5. Busy flag

Busy flag indicates that KS0108B is operating or no operating. When busy flag is high, KS0108B is in internal operating .

When busy flag is low, KS0108B can accept the data or instruction. DB7indicates busy flag of the KS0108B.



6. Display On/Off Flip-Flop

The display on/off flip-flop makes on/off the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non selective voltage appears on segment output terminals. When flip-flop is set (logic high), non selective voltage appears on segment output terminals regardless of display RAM data. The display on/off flip-flop can changes status by instruction. The display data at all segment disappear while RSTB is low.

The status of the flip-flop is output to DB5 by status read instruction.

The display on/off flip-flop synchronized by CL signal.

7. X Page Register

X page register designates pages of the internal display data RAM.

Count function is not available. An address is set by instruction.

8. Y address counter

Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by read or write operations of display data.

9. Display Data RAM

Display data RAM stores a display data for liquid crystal display. To indicate on state dot matrix of liquid crystal display , write data 1. The other way , off state, writes 0.

Display data RAM address and segment output can be controlled by ADC signal.

ADC=H => Y-address 0: S1~Y address 63: S64

ADC=L => Y-address 0: S64~Yaddress 63: S1

ADC terminal connect the V_{DD} or V_{SS} .

10. Display Start Line Register

The display start line register indicates of display data RAM to display top line of liquid crystal display.

Bit data (DB<0.5>) of the display start line set instruction is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter.

It is used for scrolling of the liquid crystal display screen.

Display Control Instruction

The display control instructions control the internal state of the KS0108B. Instruction is received from MPU to KS0108B for the display control. The following table shows various instructions.

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Read Display Date	1	1	Read data								Reads data (DB[7:0]) from display data RAM to the data bus.
Write Display Date	1	0	Write data								Writes data (DB[7:0]) into the DDRAM. After writing instruction, Y address is incremented by 1 automatically
Status Read	0	1	Bus y	0	ON/OFF	Re-set	0	0	0	0	Reads the internal status BUSY 0: Ready 1: In operation ON/OFF 0: Display ON 1: Display OFF RESET 0: Normal 1: Reset
Set Address (Y address)	0	0	0	1	Y address (0~63)						Sets the Y address at the column address counter
Set Display Start Line	0	0	1	1	Display start line (0~63)						Indicates the Display Data RAM displayed at the top of the screen.
Set Address (X address)	0	0	1	0	1	1	1	Page (0~7)			Sets the X address at the X address register.
Display On/off	0	0	0	0	1	1	1	1	1	0/1	Controls the display ON or OFF. The internal status and the DDRAM data is not affected. 0: OFF, 1: ON

1. Display On/Off

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D=0, it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

2. Set Address (Y Address)

Y address (AC0~AC5) of the display data RAM is set in the Y address counter. An address is set by instruction and increased by 1 automatically by read or write operations of display data.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

3. Set Page (X Address)

X address (AC0~AC2) of the display data RAM is set in the X address register.
Writing or reading to or from MPU is executed in this specified page until the next page is set.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	AC2	AC1	AC0

4. Display Start Line (Z Address)

Z address (AC0~AC5) of the display data RAM is set in the display start line register and displayed at the top of the screen.

When the display duty cycle is 1/64 or others (1/32~1/64), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	AC5	AC4	AC3	AC2	AC1	AC0

5. Status Read

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	BUS Y	0	ON/OFF	RESET	0	0	0	0

I BUSY

When BUSY is 1, the Chip is executing internal operation and no instructions are accepted.
When BUSY is 0, the Chip is ready to accept any instructions.

I ON/OFF

When ON/OFF is 1, the display is on.
When ON/OFF is 0, the display is off.

I RESET

When RESET is 1, the system is being initialized.
In this condition, no instructions except status read can be accepted.
When RESET is 0, initializing has finished and the system is in the usual operation condition.

6. Write Display Data

Writes data (D0~D7) into the display data RAM.
After writing instruction, Y address is increased by 1 automatically.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

7. Read Display Data

Reads data (D0~D7) from the display data RAM.
After reading instruction, Y address is increased by 1 automatically.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0